WHAT IS CLAIMED IS:

1. A magnetic random access memory in which "0" data and "1" data are associated with resistance values of a non-magnetic layer of a magnetoresistive element, the resistance values being variable depending on orientation of magnetization of a magnetic free layer and a magnetic pinned layer which sandwich the non-magnetic layer, and current is let to flow to first and second write current paths, which are provided close to the magnetoresistive element and are separated from each other, thereby producing a composite write magnetic field, changing a direction of magnetization of the free layer,

wherein the first write current path includes a channel region of an insulated-gate transistor that is disposed close to the free layer, and the transistor is controlled such that a channel current with a desired magnitude flows in the transistor.

2. The magnetic random access memory according to claim 1, wherein the transistor is connected to a write power supply that is controlled such that the channel current in one of opposite directions corresponding to write data "0" and write data "1" is caused to flow as the write current.

3. The magnetic random access memory according to claim 1, wherein gate wiring continuous with a gate electrode of the transistor is provided as the second

write current path, and when data is written to the magnetoresistive element, the gate wiring is supplied with write current in one of opposite directions in accordance with one of write data "0" and write data "1" and the transistor is controlled such that a channel current in a predetermined direction flows as write current that flows in the first write current path.

4. The magnetic random access memory according to claim 1, wherein at least a part of peripheral surfaces of a gate electrode of the transistor is coated with a magnetic material.

5. The magnetic random access memory according to claim 1, wherein the transistor is a thin-film transistor.

6. The magnetic random access memory according to claim 1, wherein the transistor further functions as a transistor for read-out cell selection.

7. The magnetic random access memory according to claim 6, further comprising first and second read-out voltage application terminals, wherein the first read-out voltage application terminal is connected to one end of the magnetoresistive element, the other end of the magnetoresistive element is connected to one of source and drain electrodes of the transistor via a gate electrode of the transistor, and the other of the source and drain electrodes is connected to

the second read-out voltage application terminal.

8. A magnetic random access memory in which "0" data and "1" data are associated with resistance values of a non-magnetic layer of a magnetoresistive element that includes a magnetic free layer and a magnetic pinned layer which sandwich the non-magnetic layer, the resistance values being variable depending on orientation of magnetization of the magnetic free layer and the magnetic pinned layer, and current is let to flow to at least one write current path, which is provided close to the magnetoresistive element, thereby producing a write magnetic field, changing a direction of magnetization of the free layer of the magnetoresistive element,

wherein the write current path includes a channel region of an insulated-gate transistor that is disposed close to the free layer of the magnetoresistive element, and the transistor is controlled such that a channel current, which generates a write magnetic field with a magnitude corresponding to a write threshold or more, flows in the transistor as a write current.

9. A magnetic random access memory comprising:

a wiring formed on a semiconductor substrate;

a plurality of tunneling magnetoresistive elements disposed along the wiring at intervals, and having a tunneling magnetoresistive effect that is obtained by

such a structure that a non-magnetic layer is sandwiched between a magnetic pinned layer and a magnetic free layer; and

a plurality of insulated-gate transistors disposed at intervals along the wiring in association with the plurality of tunneling magnetoresistive elements, each of the transistors having a part of the wiring as a gate electrode, and a channel region that is disposed close to the free layer of an associated one of the plurality of magnetoresistive elements,

wherein the transistor is controlled such that when data is written to the magnetoresistive element, a channel current with a desired magnitude flows as a part of write current.

10. The magnetic random access memory according to claim 9, wherein the free layer and the pinned layer are set to have directions of spin, which coincide with a channel width direction of the channel region of the transistor.

11. The magnetic random access memory according to claim 10, further comprising:

a word line formed to extend in the channel width direction of the channel region as a gate electrode of the transistor; and

a bit line formed such that the tunneling magnetoresistive element is sandwiched between the bit line and the word line, the bit line being disposed in

a direction perpendicular to the word line.

12. The magnetic random access memory according to claim 11, wherein at a time of data write, a magnetic field that is generated by a bit current flowing in the bit line and a magnetic field that is generated by the channel current are combined to produce a write magnetic field, and the write magnetic field controls the direction of spin of the free layer.

13. The magnetic random access memory according to claim 12, wherein at a time of data read-out, a read-out circuit is formed between the word line and the bit line via the tunneling magnetoresistive element.

14. The magnetic random access memory according to claim 9, further comprising:

a word line formed to extend in a channel length direction of the channel region as a gate electrode of the transistor; and

a bit line formed such that the tunneling magnetoresistive element is sandwiched between the bit line and the word line, the bit line being disposed in a direction perpendicular to the word line.

15. The magnetic random access memory according to claim 14, wherein at a time of data write and data erasure, a magnetic field that is generated by a bit current flowing in the bit line and a magnetic field that is generated by the channel current are combined to produce a write magnetic field, and the write

magnetic field controls the direction of spin of the free layer.

16. The magnetic random access memory according to claim 15, wherein at a time of data read-out, a read-out circuit is formed between the word line and the bit line via the tunneling magnetoresistive element.

17. The magnetic random access memory according to claim 9, wherein the free layer and the pinned layer are set to have directions of spin, which coincide with a channel length direction of the channel region of the transistor.

18. The magnetic random access memory according to claim 17, further comprising:

a word line formed to extend in the channel length direction of the channel region as a gate electrode of the transistor; and

a bit line formed such that the tunneling magnetoresistive element is sandwiched between the bit line and the word line, the bit line being disposed in a direction perpendicular to the word line.

19. The magnetic random access memory according to claim 18, wherein at a time of data write and data erasure, a magnetic field that is generated by a bit current flowing in the bit line and a magnetic field that is generated by the channel current are combined to produce a write magnetic field, and the write

magnetic field controls the direction of spin of the free layer.

20. The magnetic random access memory according to claim 18, wherein at a time of data read-out, a read-out circuit is formed between the word line and the bit line via the tunneling magnetoresistive element.